an input terminal for supplying an input signal to a circuit to be protected;

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

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a second well region of the first conductivity type formed in the principal surface area of said semiconductor substrate;

third and fourth well regions of the second conductivity type formed in said second well region and forming a second lateral bipolar transistor with a portion of said second well region serving as a base, bottoms of said third and fourth well regions forming a PN junction with said second well or with said semiconductor substrate; and

a circuit formed in said semiconductor substrate and connected to said input terminal;

wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region, said first lateral bipolar transistor operating without a fixed base bias, and said fourth well region and the base of the second lateral bipolar transistor are connected to one reference potential node.

5. (Twice Amended) An input protection circuit comprising:

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an input terminal for supplying an input signal to a circuit to be protected;

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

second and third well regions of a second conductivity type formed in the principal surface area of said semiconductor substrate, said second and third well regions forming a second lateral bipolar transistor with a portion of said semiconductor substrate serving as a base;

a circuit formed in said semiconductor substrate and connected to said input terminal;

wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said second well region, said first lateral bipolar transistor operating without a fixed base bias, and said third well region and the base of the second lateral bipolar transistor are connected to one reference potential node.

23. (New) The input protection circuit of claim 1, wherein the second lateral bipolar transistor is turned on to protect the input protection circuit when a high voltage of a first polarity, the first polarity corresponding to the first conductivity type, is applied

to the input terminal.

24. (New) The input protection circuit of claim 1, wherein the first lateral bipolar transistor is turned on to protect the input protection circuit when a high voltage of a second polarity, the second polarity corresponding to the second conductivity type, is applied to the input terminal.

25. (New) The input protection circuit of claim 5, wherein the second lateral bipolar transistor is turned on to protect the input protection circuit when a high voltage of a first polarity, the first polarity corresponding to the first conductivity type, is applied to the input terminal.

26. (New) The input protection circuit of claim 5, wherein the first lateral bipolar transistor is turned on to protect the input protection circuit when a high voltage of a second polarity, the second polarity corresponding to the second conductivity type, is applied to the input terminal.